

UNITED STATES PATENT APPLICATION

of

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for

EDGE POWER DETECTOR/CONTROLLER

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EDGE POWER DETECTOR/CONTROLLER

BACKGROUND OF THE INVENTION

The invention relates to the field of RF power detectors and controllers, and in particular to RF power detectors and controllers used in mobile handset terminals for wireless applications.

5 The rollout of the new 2.5 and 3G wireless systems presents unique challenges to mobile handset designers. In order to reap the full benefit of expanded capacity and data bandwidth, the new handsets must work on both the new systems as well as the old. One of these new systems is the so-called Enhanced Data Rates for Global Evolution (EDGE). The EDGE standard is an extension of the Global System for Mobile Communications (GSM) standard.

10 EDGE increases the data rate over that available with GSM by sending more bits per RF burst. More bits are sent in EDGE by using a modulation scheme based on 8-phase shift keying (8-PSK), which provides an increase over GSM's Gaussian minimum shift keying (GMSK) modulation format. In the EDGE modulation scheme, the 8-PSK constellation is rotated $3\pi/8$ radians every symbol period to avoid the problems associated with zero crossings. In contrast to 15 GMSK's constant amplitude envelope, the added rotation factor in the EDGE modulation scheme results in a non-constant amplitude envelope. This non-constant amplitude envelope presents some difficulties with regard to RF power control. These problems are exacerbated by the desire to have one transmitter that can be used for both the GSM and EDGE standards.

Figure 1 shows a prior art power detection and control system 100 for GSM systems. 20 GSM constant envelope signals are input to and amplified by a power amplifier (PA) 102. Signals output by power amplifier 102 are coupled by a directional coupler 108 into some form

of demodulating detector 104, typically a logarithmic amplifier (log amp), which translates the power of the output signals into a voltage. Figure 2 shows the output 200 of demodulating log amp 104 when a GSM signal 202 is applied at the input. As shown in figure 2, the voltage 200 output by log amp 104 is a DC voltage because GSM signals have a constant amplitude
5 envelope. The DC output of log amp 104 is then compared to a ramp control signal using a high gain, frequency limited differential amplifier 106. Based upon the comparison, differential amplifier 106 outputs an error signal, which is filtered by a filter capacitor 107 (amplifier 102 is configured as an integrator) to create a PA ramp voltage that is used to control the power output of PA 102. This creates a closed loop system that will set the output power to a level defined by the ramp control signal. The system is defined by the power control slope in dB/V and the 0V intercept point in dBm. The frequency response of this closed loop system must be fast enough to provide an adequate rise time, and slow enough to avoid ringing or instability.

Some unique problems arise when an EDGE signal having a non-constant amplitude envelope is applied to the GSM control loop 100. The EDGE system standard requires that PA 102 ramp up and down with the same speed as for GSM (28uS). Thus, the loop must have a response faster than 35 kHz. However, unlike the GSM signal, the EDGE signal contains an AM component resulting from the non-constant amplitude envelope. Logarithmic amplifier 104 will detect this modulation and vary the output DC voltage accordingly. This is illustrated in figure 3, which shows the output 300 of demodulating log amp 104 when an EDGE signal 302 is applied at the input. As shown in figure 3, the voltage 300 output by demodulating log amp 104 has a voltage ripple component that results from the non-constant amplitude envelope, in
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addition to the constant DC voltage component. The resulting voltage ripple results in as much as a 20dB variation in amplitude. Because the DC voltage is varied according to the AM component, the negative feedback of the closed loop system will work to eliminate the AM information in the EDGE signal.

5 Several methods for solving this problem have been proposed. First, two different filters could be used. A fast filter is used for the power ramping section of the signal, and a second, slower filter is switched in when the AM modulation begins. This solution will still allow some AM variation to leak into the loop since the filter will require some amount of time to create an average and settle. Another approach is to remove the second filter and simply hold the DC voltage constant during the AM modulation phase. This track and hold function will not have the same problem with settling time and no AM ripple will leak into the loop. However, the system will be running open-loop while the hold function is engaged. Thus, no corrections can be made to the PA output power during the RF burst to compensate for external influences (battery fluctuations, temperature, etc.). The finite nature of the data is another problem. Only 15 102 symbols of data are transmitted per frame. This small sample size means that there will be variations in the number and type of phase transitions per frame thus changing the peak to average ratio of the signal and the resulting average power per frame. An open loop system will not be able to adjust for these variations.

SUMMARY OF THE INVENTION

20 The present invention provides a power detector/controller for signals having modulation scheme with a non-constant amplitude envelope. The power detector/controller comprises a

power amplifier, an output demodulating detector and a summing junction. The power amplifier has an input to receive an input signal with non-constant amplitude envelope and an output to output an amplified input signal. A power amplifier control signal controls either output power or gain of the power amplifier. The output demodulating detector is coupled to the output of the power amplifier to generate a feedback signal proportional to the amplified input signal's power. The feedback signal includes an AM variation due to the non-constant amplitude envelope. The summing junction receives the feedback signal, a ramp control signal that indicates either a target gain or target output power of the power amplifier, and an AM variation signal that represents the AM variation in the power of the input signal due to the non-constant amplitude envelope. The summing junction combines the feedback signal, the ramp control signal and AM variation signal to produce the power amplifier control signal such that the power amplifier control signal substantially free of any AM variation due to the non-constant envelope.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a prior art power measurement and control system for GSM systems.

Figure 2 shows the output of a demodulating log-amp with a GSM signal applied.

Figure 3 shows the output of a demodulating log-amp with an EDGE signal applied.

5 Figure 4 conceptually illustrates a power detector/controller according to the present invention.

Figure 5 illustrates one embodiment of a power detector/controller according to the present invention.

Figure 6 shows another embodiment of a power detector/controller according to the present invention.

Figure 7 illustrates another embodiment of a power detector/controller according to the present invention.

Figure 8a illustrates an implementation of the embodiment shown in figure 7 using an AD8315 log amplifier/controller.

Figure 8b illustrates a schematic of the AD8315 log amplifier/controller.

15 Figure 9 illustrates an implementation of the embodiment shown in figure 7 using an AD8302.

Figure 10 illustrates another implementation using discrete log-amps.

Figure 11 shows an embodiment of the present invention where the AM variation of the envelope is provided from the base-band processor, which eliminates the need for the input demodulating detector.

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides a closed-loop power detector/controller for wireless systems employing a non-constant amplitude envelope modulation scheme. Any AM component in the closed loop feedback signal is eliminated via feed-forward cancellation of the envelope signal. Generally, a signal representative of the AM variation in the non-constant amplitude envelope signals prior to amplification is obtained. This AM variation signal is then used to cancel any AM component in the feedback signal resulting from the non-constant envelope so that a PA control signal that has no-AM-component, only the desired ramp profile, can be created.

In addition to setting the output power, this control circuit also improves the linearity of the PA. Some amplitude distortion may be present due to non-linearities present in the PA. The difference between the input AM component and the output AM component is known as the amplitude distortion. Even though the AM component in the feedback signal due to a non-constant envelope is cancelled by feedforward, this amplitude distortion is not, and is therefore introduced as negative feedback at the PA. Thus, the corrective signal to the PA will respond to the amplitude distortion, resulting in some degree of improvement in the linearity of the PA. This side benefit of the detector can be further exploited by those familiar with polar loop feedback systems to create a highly linear amplifier from otherwise saturated, or non-linear amplifiers. However, even if this residual AM ripple is not further exploited for linearization, its presence will not interfere with the operation of the closed loop power control.

A power detector/controller 400 according to the present invention is conceptually illustrated in figure 4. As shown in figure 4, a PA 402 amplifies input RF signals. PA 402 is either a gain controlled PA or a power controlled PA. When PA 402 is a power controlled PA, its output power is controlled by a control signal, V_{apc} . When it is a gain controlled PA, its gain is controlled by the control signal V_{apc} .

5 An output coupler 408 couples a portion of the output RF signal to an output demodulating detector 404. Demodulating detector 404 translates the coupled output RF signal into a feedback signal proportional-to-the-power in the RF output signal. This feedback signal is output to summing junction 405.

Summing junction 405 also receives the ramp control signal. The ramp control signal is proportional to either the target gain of PA 402 or the target output power of PA 402, depending upon whether PA 402 is power controlled or gain controlled. Any PA can be subject to gain control or power control depending on how the detectors are configured.

15 In addition to the feedback signal and ramp control signal, summing junction 405 receives an AM variation signal that represents the AM variation in the input signal power resulting from the non-constant envelope. Any envelope variation that is present on the detected signal at the output of PA 402 is also present on the input signal to the PA 402. Thus, by obtaining the AM variation in the input signal power, the AM variation can be cancelled from the feedback signal obtained from the output.

20 To obtain the AM variation of the input signal power, an input demodulating detector 414 is used. Input demodulating detector 414 and output demodulating detector 404 are balanced

detectors. They can be logarithmic detectors or linear detectors. Input demodulating detector 418 receives a portion of the input RF signal from coupler 418 via phase shifter 416. Phase shifter 416 adds a delay to the coupled input signal so that the AM variation from the input signal is aligned with the AM variation from the output signal to ensure cancellation of the AM variation. Input demodulating detector 414 receives the delayed, coupled input signal and translates it into a signal proportional to the power in the input RF signal. Demodulating detector 414 outputs this AM variation signal to summing junction 405.

As an alternative to using an input demodulating detector 414 to obtain the AM variation, the AM variation signal is obtained directly from the base-band processor.

At summing junction 405, conditioning of the AM variation signal is performed, if needed for the control loop type (i.e., power or gain control). Conditioning circuitry in summing junction 405 removes the DC component from the AM variation signal depending upon whether gain or power is controlled. When power control is desired, the DC component is removed to effectuate a power control loop. When gain control is desired, the DC component is not removed. It should be noted that power control can also be effectuated without removal of the DC component, as will be further described below. To remove the DC component, the output of demodulating detector 414 is ac-coupled, or otherwise high-pass filtered.

Also, conditioning of the AM variation signal is performed at summing junction 405 if needed to ensure cancellation. For instance, if necessary to ensure cancellation, conditioning circuitry adjusts the amplitude of the AM variation in the output of demodulating detector 414. When balanced demodulating detectors 404 and 414 are logarithmic amplifiers, the amplitude of

the AM variation output by both is substantially the same regardless of the gain of the PA. In this case, the amplitude does not need adjusting. However, when the demodulating detectors 404 and 414 are linear detectors then the amplitudes are not substantially the same and the amplitude of the AM variation in the signal output by demodulating detector 414 needs adjusted to ensure 5 amplitude cancellation.

After any necessary conditioning, the conditioned AM variation signal, ramp control signal, and feedback signal are then combined in summing junction 405 so as to cancel any AM variation in the signals that results from the AM component in the input signals, and to produce an error signal, which is filtered to create a PA control signal, V_{apc} , that is used to control the output of PA 402. It should be noted that, in practice, it is difficult to achieve a perfect phase and amplitude match between the AM variation signal and the AM variation in the feedback signal for cancellation. However, it is not necessary for the match to be exact, and cancellation on the order of -10dB is adequate.

It should also be noted that even though V_{apc} is shown as a DC voltage, this is illustrative 15 to indicate the AM variation has been removed. As a result of the filtering in practice, a ramped profile will actually result. The ramped profile typically takes the form of a raised cosine.

Advantageously, a power detector/controller according to the present invention supports not only non-constant envelope signals, such as those in EDGE, but also constant envelope signals, such as those in GSM. Hence, only a single power detector/ controller according to the 20 present invention needs to be used in wireless handsets designed to operate on both GSM and EDGE systems.

Figure 5 illustrates an embodiment of a power detector/controller 500 according to the present invention in which the summing junction comprises a differential amplifier 506, a sum node 510, a filter capacitor 507, an ac-coupling capacitor (not shown), and a variable gain amplifier (VGA) 512. In this embodiment, demodulating detectors 514 and 504 are linear amplifiers. 5 detectors.

The input and output of a PA 502 are respectively coupled to balance demodulating detectors 514 and 504 respectively. A directional coupler 518 couples the input-to-input demodulating detector 514 via a phase shifter 516. Phase shifter 516 adds a delay to the input signal to align the input and output signals so that an AM variation signal determined from the input and a feedback signal determined from the output are aligned. A directional coupler 508 couples the output-to-output demodulating detector 504.

Demodulating detector 514 translates the power of the input signal into a voltage that includes any voltage ripple resulting when input signals have a non-constant amplitude envelope. While not shown, the output of input detector 514 is ac-coupled to VGA 512 with an ac-coupling capacitor to remove the DC component from the voltage. In this configuration, the circuit provides power control. However, if the initial, un-amplified DC component of the signal from detector 514 were preserved in the signal output by VGA 512, then the circuit would provide gain control. VGA 512 adjusts the amplitude of the ripple voltage according to the ramp control signal to ensure amplitude cancellation. The VGA 512 outputs the conditioned AM variation signal to sum node 510.

Similarly, output demodulating detector 504 translates the power of the output signal into a voltage that also includes any voltage ripple resulting when input signals have a non-constant amplitude envelope. This feedback voltage is input to the negative input of differential amplifier 506, while the ramp control signal is input to the positive input. The differential amplifier 506 outputs an error signal for controlling PA 502, which, however, still contains the voltage ripple due to the AM component.

The AM variation signal from VGA 512 is added to the error signal from differential amplifier 506 at sum node 510 to eliminate the voltage ripple from the error signal. Filter capacitor 507 filters the output of sum node 510, which results in a control signal, V_{apc} , with a ramped profile that controls the gain of PA 502.

Figure 6 shows another embodiment of a power detector/controller 600 according to the present invention in which the summing junction comprises a differential amplifier 606, a multiplication node 610, and a filter capacitor 607 and appropriate conditioning circuitry (not shown). In this embodiment, demodulating detectors 604 and 614 are linear detectors. The operation of this embodiment is essentially the same as that of figure 5, except, however, for where the AM variation is removed.

As shown, directional coupler 618 couples the input signal to input demodulating detector 614 via phase shifter 616, which delays the input signal to align it to the output signal, similar to the embodiment of figure 5. Input demodulating detector 614 translates the power of the input signal into a voltage that includes any voltage ripple resulting when input signals have a non-constant amplitude envelope. While not shown, as with the embodiment of figure 5,

appropriate circuitry removes any DC component subsequent to input demodulating detector 614 and the amplitude of the ripple voltage is adjusted to ensure cancellation. The resulting signal is then combined with the ramp control voltage at multiplication node 610 to generate a composite ramp control/AM variation signal. This composite signal is provided to positive input of 5 differential amplifier 606.

A directional coupler 608 couples the output of PA 602 to output demodulating detector 604. Output demodulating detector 604 translates the power of the output signal into a voltage that includes any voltage ripple resulting when input signals have a non-constant amplitude envelope. This signal is applied to the negative input of differential amplifier 606.

Differential amplifier 606 generates the PA control, V_{apc} , signal by subtracting the power signal output by output detector 604 from the composite ramp control/AM variation signal to generate an error signal without AM variation. Differential amplifier 606 is set up as an integrator with filter capacitor 607 to filter the error signal to produce a ramped profile, which is applied as the PA control, V_{apc} .

15 Figure 7 illustrates another embodiment of a power detector/controller 700 according to the present invention in which the summing junction comprises a differential amplifier 706, a sum node 710, and a filter capacitor 707, and an ac-coupling capacitor 720. In this embodiment, demodulating detectors 714 and 704 are logarithmic amplifiers.

In the same manner as described above, a 30 dB directional coupler 718 couples the input signal to input log amp 714 via phase shifter 716, which delays the input signal to align it to the 20 output signal. Input log amp 714 translates the power of the input signal into a voltage that

includes any voltage ripple resulting when input signals have a non-constant amplitude envelope.

The output of input log amp 714 is ac-coupled via capacitor 720 to remove its dc component.

This signal is then added to the ramp control signal, V_{SET} , at summing node 710 to create a composite ramp control/AM variation signal. The composite signal is then applied to the

5 positive input of differential amplifier 706, which is configured as a difference integrator.

A 30 dB directional coupler 708 couples the output to 30 dB attenuator 722, which

attenuates the output signal before providing it to output log amp 704. While not necessary,

~~when using balance logarithmic demodulating detectors, it is advantageous to use attenuator 722~~

to make the amplitudes of the signals input to demodulating detectors 716 and 722 similar in

magnitude. Thus for example, when the maximum output power of PA 702 is 30 dB, a 30 dB

attenuator is used for attenuator 722 to make the inputs similar in magnitude. Of course, other set points can be used, and, ideally, attenuator 722 would exactly attenuate the power of the

50 signal from directional coupler 708 by the same amount that PA 702 is outputting.

Output log amp 704 translates the power of the output signal into a voltage that includes

any voltage ripple resulting when input signals have a non-constant amplitude envelope. This

15 signal is applied to the negative input of differential amplifier 706. Differential amplifier 706

then compares the composite signal to the output of log amp 704. Any differences in these

signals will result in a corrective signal V_{apc} being applied to the PA's V_{apc} input.

Figure 8a illustrates an implementation of the embodiment shown in figure 7 using an

20 AD8315 log amplifier/controller from Analog Devices. As shown in figure 8b, the AD8315 log

amplifier/controller 804 incorporates a logarithmic amplifier RF detection subsystem and an

error amplifier/integrator section 805. The AD8315 is, therefore, is used to implement output log amp 704 and amplifier/integrator 706. As shown in figure 8a, the sum of the ramp control signal, V_{SET} , and the ac-coupled signal from input log amp 814, is applied to the V_{SET} input of the AD8315. The output of the AD8315 (V_{apc}) drives the V_{apc} input of the PA.

5 The embodiment of figure 7 can also be implemented using an AD8302 Gain-Phase

detector from Analog Devices. An AD8302 comprises two log amps and a sum node. Figure 9 illustrates an implementation of the embodiment of figure 7 using an AD8302. The input signal to PA 902 and the output signal from PA 902 are sampled using 30dB directional couplers 918 and 908, respectively. The coupled input signal is delayed by phase shifter 916 so as to align the AM variation in the input of PA 902 to the AM variation in the output of PA 902. The delayed input signal is provided from phase shifter 916 to input log amp 914 of AD8302 820. Log amp 914 translates the power of the delayed input signal into a current, I_{log1} , that includes any current ripple resulting when input signals have a non-constant amplitude envelope.

Attenuator 922 attenuates the coupled output signal by 30 dB to facilitate input signal balancing to the AD8302 920. The attenuated output signal is provided from attenuator 922 to output log amp 904 of AD8302 920. Log amp 904 translates the power of the attenuated output signal into a current, I_{log2} , that includes any current ripple resulting when input signals have a non-constant amplitude envelope.

20 The ramp control voltage, which corresponds to the desired gain of PA 902, is applied to the V_{SET} input of AD8302 920. This voltage is converted to a current, I_{set} , by a voltage-to-current converter 924 inside AD8302 920. This current, I_{SET} , is summed at node 930 with the

currents, $I_{\log 1}$ and $I_{\log 2}$, from the input log amps 914 and 904. Node 930 sinks I_{SET} and $I_{\log 1}$, while sourcing $I_{\log 2}$. This causes the simultaneous subtraction of $I_{\log 2}$ (i.e., output power signal) from the sum of $I_{\log 1}$ and I_{SET} (i.e., the AM variation and ramp control signal). This causes cancellation of the AM variation. Any residual error current at node 930 will either charge or discharge filter capacitor 907 which will either increase or decrease the voltage V_{apc} signal 5 output by voltage buffer 928 to PA 902. This embodiment results in the dB gain of PA 902 being proportional to the voltage of the V_{SET} signal.

Figure 10 illustrates another embodiment using discrete-log amps in which power control is provided instead of gain control. This embodiment provides a means for power control without having to AC couple the detected input signal.

For gain control only circuits, if the input power to the PA is well controlled, then the output power will also be well controlled. However, if the input power varies, the output power will also vary. Therefore, it is advantageous to perform power control.

Output power control is achieved by tapping off the signal from output log amp 1004 before it is applied to sum node 1030 and comparing it to the ramp control signal, V_{set} , using an operational amplifier 1025. The output of amplifier 1025, when the system is in equilibrium, is equal to the voltage from output log amp 1004 minus the voltage from input log amp 1014. If the output from input log amp 1014 changes, the output of amplifier 1025 will change (changing the gain set point) but the voltage from output log amp 1004 will remain the same, thereby 15 keeping the output power constant.

Some filtering of the signal fed to amplifier 1025 from output log amp 1004 is needed to prevent the op-amp from responding to the fast changes in the envelope of the output signal. Therefore, low pass filter 1026 filters this signal before it is input to amplifier 1025. Filter 1026 introduces a delay in the signal from detector 1004 to op-amp 1025, which causes the initial response of the circuit to set the gain of the amplifier. The second control loop, formed by low pass filter 1026 and op-amp 1025, takes over after a delay proportional to the bandwidth of filter 1026 and corrects the output power level. Filter 1026 is disabled during ramping in order to speed the response of the power control when no AM signal is present and enabled during burst transmission. Therefore, in this implementation, the summing junction comprises operational amplifier 1025, sum node 1030, low pass filter 1026 and error amplifier/integrator 1028.

In another embodiment of the present invention, the input demodulating detector is eliminated by obtaining a signal representative of the AM variation directly from the base-band signal. A power detector/controller 1100 according to this embodiment is shown in Figure 11. The AM variation of the signal is provided by the base-band processor in the wireless handset and summed with the ramp control signal at summing node 1110. Otherwise, power detector/controller 1100 operates the same as power controller/detector 600 of figure 6. The signal from the base-band processor should be properly conditioned to compare correctly with the output detected signal. That is, if a logarithmic detector is used at the output, then the base-band processor should provide a logarithmic signal, and if a linear detector is used, then the base-band processor should provide a linear signal with the appropriate scaling.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention. While some signals have been described as voltages, and others as currents, one of skill in the art would appreciate that the signals described could be either and are not limited to the form described.

What is claimed is: